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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/506,371	09/02/2004	Isao Sasaki	NEC 02P211	9956

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EXAMINER	
PERVAN, MICHAEL	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
03/05/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/506,371	SASAKI ET AL.	
	Examiner	Art Unit	
	Michael Pervan	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) *27-42* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,13-16,26,44 and 45* is/are rejected.

7)☒ Claim(s) *4-12,17-25 and 43* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed December 10, 2009 have been fully considered but they are not persuasive.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., compensating for the variation in characteristics in the drive transistor) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant (on pages 2-3 of argument) argues that Dingwall and Ikeda together do not disclose the connection relationship of claim 44. Examiner respectfully disagrees.

Dingwall discloses the same connection relationships as that of claim 44 except the junction node of the capacitor is not between the driving transistor and the pixel display element, but rather is located between the pixel display element and ground. Ikeda discloses having the junction node of the capacitor be between the driving transistor and the pixel display element. Although, Ikeda has the pixel display element and the driving transistor connected in parallel, it was only used to show that a junction node of a capacitor can be located between a pixel display element and a driving transistor. As a result, Dingwall and Ikeda still read on the claims and the rejection stands.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 13-16, 26 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall (US 5,903,246) in view of Tanaka et al (US 2001/0007447).

In regards to claims 1, 14 and 45, Dingwall discloses an image display apparatus comprising (Fig. 2):

a pixel having a drive transistor (TR1-480) and a pixel display element (P1-480) which are electrically connected in series between a first power line (VDD) and a second power line (ground), a holding capacitor (C1-480) electrically connected to a gate electrode of said drive transistor, and a selection transistor (T1-480) electrically connected between a signal line (ROW1-480) and the gate electrode of said drive transistor; and

a controller for turning on said selection transistor thereby to write gradation pixel data in said holding capacitor from said signal line (It is inherent that there would be a ROW driver for activating the selection transistor), discharging charges of the gradation pixel data written in said holding capacitor through said drive transistor for a predetermined time (col. 5, lines 25-45).

Dingwall does not disclose the predetermined time being less than a frame time and thereafter floating the gate electrode of said drive transistor thereby to hold the charges of the gradation pixel data stored in said holding capacitor.

Tanaka discloses the predetermined time being less than a frame time (paragraphs 40-41; the frame time includes a writing period and a driving period. It is obvious that discharging occurs during the driving period. Therefore the predetermined time (driving period) is less than a frame time) and thereafter floating the gate electrode of said drive transistor thereby to hold the charges of the gradation pixel data stored in said holding capacitor (paragraph 32).

It would have been obvious at the time of invention to modify Dingwall with the teachings of Tanaka, having a predetermined time being less than a frame time and floating the gate electrode of said drive transistor, because it would reduce power consumption (Tanaka: paragraph 6)

In regards to claims 2 and 15, Dingwall discloses the image display apparatus according to claim 1, further comprising:

a display panel having a plurality of signal lines (COL1-560) to which corresponding gradation pixel data are applied and a plurality of scanning lines (ROW1-480) to which scanning signals are applied, said pixel being positioned at each of points of intersection between said signal lines and said scanning lines (Fig. 2);

a signal line driver (digital current source) for applying said gradation pixel data to said signal lines based on a pixel input signal (col. 5, lines 3-7); and

a scanning line driver for applying said scanning signals to said scanning lines (It is inherent that there would be a ROW driver for activating the selection transistor);

wherein said selection transistor has a first drain electrode, a first source electrode, and a first gate electrode, said drive transistor has a second drain electrode, a second source electrode, and a second gate electrode, said holding capacitor holds a voltage between said second gate electrode and said second source electrode, and said pixel display element has a first electrode and a second electrode (Fig. 2);

wherein said first drain electrode/said first source electrode is connected to said signal line, said first source electrode/said first drain electrode is connected to said second gate electrode, said first gate electrode is connected to said scanning line, and said selection transistor performs on/off control of a conduction state between said signal line and said second gate electrode based on said scanning signal (Fig. 2);

wherein said first power line is connected to said second drain electrode, said second source electrode is connected to said first electrode, and said drive transistor passes an output current controlled based on a voltage held by said holding capacitor from said second source electrode to said first electrode (Fig. 2 and col. 5, lines 25-45); and

wherein said second power line is connected to said second electrode, and said pixel display element displays a pixel at a gradation based on said output current of said drive transistor (Fig. 2 and col. 5, lines 25-45).

In regards to claims 3 and 16, Dingwall discloses the image display apparatus according to claim 2, wherein said scanning signals are applied to said scanning lines in a preset sequence (col. 5, lines 28-34).

In regards to claims 13 and 26, Dingwall discloses the image display apparatus according to claim 1, wherein said pixel display element comprises an organic electroluminescence element (col. 2, line 66-col. 3, line 5).

4. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall (US 5,903,246) in view of Ikeda (US 5,714,968).

In regards to claim 44, Dingwall discloses an image display apparatus comprising:

a pixel having a drive transistor (TR1-480) and a pixel display element (P1-480) which are electrically connected in a series between a first power line (VDD) and a second power line (ground), a holding capacitor (C1-480) electrically connected between a gate electrode of said drive transistor and a junction node, and a selection transistor (T1-480) electrically connected between a signal line (COL_1-560) and the gate electrode of said drive transistor (Fig. 2).

Dingwall does not disclose said junction node being of between said pixel display element and a source electrode of said drive transistor.

Ikeda discloses said junction node being of between said pixel display element and a source electrode of said drive transistor (Fig. 10; as can be seen from the

drawing, capacitors (26,27) are connected to the gates of drive transistors (22, 23) and to a node which is between the drive transistor and EL elements (20, 21)).

It would have been obvious at the time of invention to modify Dingwall with the teachings of Ikeda, having a capacitor connected between a gate of a drive transistor and a node between a source of the drive transistor and the pixel, because it allows the light emitting element to be driven at a stable light intensity irrespective of the characteristics of the drive transistor (Ikeda: col. 2, lines 5-6).

Allowable Subject Matter

5. Claims 4-12, 17-25 and 43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claims 4-12, 17-25 and 43 recite among other features a resetting signal line and a resetting transistor.

The prior art does not teach or suggest the above limitations.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629

Feb. 26, 2010